FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		SOEI/0016
		U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR) 10/030525
INTERNATIONAL APPLICATION NO. PCT/JP00/02914	INTERNATIONAL FILING DATE 2 MAY 2000 (02.05.2000)	PRIORITY DATE CLAIMED 7 MAY 1999 (07.05.1999)

TITLE OF INVENTION
METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

APPLICANT(S) FOR DO/EO/US
TAMITANI, ET AL.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)). (unexecuted)
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ **A FIRST** preliminary amendment.
16. ☐ **A SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information: Letter of Transmittal

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/030525	PCT/JP00/02914	SOEI/0016

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

	CALCULATIONS PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$890.00**
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	18 - 20 =	0	x $18.00	**$0.00**
Independent claims	4 - 3 =	1	x $84.00	**$84.00**
Multiple Dependent Claims (**check if applicable**).			☐	**$0.00**
TOTAL OF ABOVE CALCULATIONS			=	**$974.00**
☐ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**
SUBTOTAL			=	**$974.00**
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**
TOTAL NATIONAL FEE			=	**$974.00**
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (**check if applicable**).			☐	**$0.00**
TOTAL FEES ENCLOSED			=	**$974.00**
			Amount to be: refunded	$
			charged	$

a. ☐ A check in the amount of _____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. **200782/SOEI16** in the amount of **$974.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **200782SOEI16** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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REGISTRATION NUMBER

7 NOVEMBER 2001
DATE

3/prts

DESCRIPTION

Method of Manufacturing Semiconductor Device

Technical Field

The present invention relates to a method of manufacturing a semiconductor device, and the semiconductor device.

Background Art

Plasma etching has been employed in forming metal wiring of semiconductor integrated circuits. For example, when an aluminum film (Al film) or aluminum alloy film (Al alloy film) is plasma-etched, a gas containing Cl atoms, such as Cl_2, BCl_3, or CCl_4, can be used as an etching gas. In the plasma etching of a metal film, photoresist can be used as mask material. Between the metal film and the photoresist film, a Ti system film, such as a TiN film, can be provided to act as an antireflection film.

Disclosure of the Invention

Such an etching technique is used when semiconductor integrated circuits is made on a semiconductor substrate. Some of these semiconductor integrated circuits include metal-insulator-semiconductor type semiconductor devices, each having a control electrode. In manufacturing these devices, the inventors found the following phenomena: the control electrodes of the semiconductor devices may be broken down; that the breakdown voltage of the semiconductor devices may be deteriorated.

The inventors noted these phenomena. In order to preventing the occurrence of the phenomena, engineers have taken measures, such as the change of the relevant etching recipes and etching apparatuses. However, the engineers have not always obtained the satisfactory improvement in the resulting shapes formed by etching and the process margins provided thereby. Hence, the inventors have found a problem that further improvement concerning the etching is required in the near future in order to manufacture much finer integrated circuits.

Therefore, it is an object of the present invention to provide a method of manufacturing a semiconductor device having a control electrode and the semiconductor device formed by the method, the method being capable of reducing the occurrence of the breakdown and deterioration of the control electrode in forming a metal wiring on the semiconductor device.

The inventors carried out various studies in order to achieve this object and thought that the above defects may occur in MIS semiconductor devices during the etching process due to the discharging occurred in the insulating film between the control electrodes and the semiconductor substrate, so that the insulating film is broke or deteriorated. The inventors noted that the defects may have been caused by charging up the control electrodes when the metal wiring film is being etched. The reason is as follows: a high

electric field may be exerted on the gate insulating film due to the charging-up of the control electrodes during the etching process.

The inventors thought that there were a number of ways employable for lowering the charge of the control electrodes during the etching process as follows: the change of etching recipes and the modification of the etching apparatus. Most of these ways have already been studied. Hence, the inventors tried to find another solution to reduce the amount of the charges itself and have eventually obtained the present invention configured as follows.

In a method of manufacturing a semiconductor device in accordance with the present invention, a metal wiring of a predetermined pattern is formed so as to be connected through a conduction path to a control electrode on an insulating layer formed on a substrate. This method comprises the steps of: forming a metal film; forming, on the metal layer, a hard mask having the predetermined pattern and containing a silicon system inorganic insulating film, the hard mask having a film thickness of at least 150 nm but not greater than 300 nm; and etching the metal film with the hard mask by an etching gas to form the metal wiring of the predetermined pattern.

The amount of residual electric charge electrifying the metal film can be lowered in the step of forming the metal wiring. The lowering of the charge prevents the

occurrence of the breakdown and deterioration of the insulating layer due to the electrified charge flowing into the control electrode.

The semiconductor device manufacturing method in accordance with the present invention relates to a method of manufacturing a semiconductor device having a predetermined pattern of metal wiring. This method comprises the steps of: forming, on an insulating layer, a control electrode for a metal-insulator-semiconductor type device; forming a metal film, the metal film being connected via a conduction path to the control electrode; forming, on the metal film, a hard mask with a film thickness of at least 150 nm but not greater than 300 nm having the predetermined pattern and containing a silicon system inorganic insulating film; and etching the metal film with the hard mask by an etching gas to form the metal wiring of the predetermined pattern.

The hard mask is thus employed as a mask instead of the photoresist mask in forming a wiring layer having a conduction path to the control electrode. The hard mask allows the reduction of the initial film thickness of an etching mask required to etch a metal film. Therefore, the volume of the mask can be reduced, so that the amount of the capturing electric charge is decreased in the mask during the etching process. Therefore, the amount of the electrified charge in the mask can be also reduced. This

reduction lowers a voltage applied between the control electrode and the substrate.

The inventors further carried out detailed studies and have found that another aspect. The following features relating to the present invention can be combined with the invention mentioned above. Also, the following features relating to the present invention can be combined with each other arbitrarily, whereby the combined invention can obtain not only the advantages and functions of the respective features, but also advantages and functions arising from combined features.

The inventors have found that a preferable film thickness of the hard mask falls within the range of at least 150 nm but not greater than 300 nm in order to reliably form the metal wiring by etching. The inventors have also found that a more preferable film thickness of the hard mask falls within the range of at least 180 nm but not greater than 230 nm.

In the method of manufacturing a semiconductor device in accordance with the present invention, the hard mask may contain a silicon system inorganic film, such as a silicon oxide film. This film of the hard mask acts as an insulating film for insulating metal wiring formed in later steps. Thus, it is not necessary to remove the hard mask. For example, at least one of SiO_2, SiN, SiOF, and SiON films can be employed as the silicon system inorganic film.

In the semiconductor device manufacturing method in accordance with the present invention, at least one of an Al film and an Al alloy film can be employed as the metal film. Further, at least one of a tungsten film and a copper film can be also employed.

Preferably, in the semiconductor device manufacturing method in accordance with the present invention, the metal film is etched by an etching gas containing Cl.

The semiconductor device manufacturing method in accordance with the present invention further comprises the step of forming a barrier metal film. The semiconductor device manufacturing method in accordance with the present invention further comprises the step of etching the barrier metal film with the hard mask. The semiconductor device manufacturing method in accordance with the present invention further comprises the step of forming an antireflection film on the metal film prior to forming the hard mask. The semiconductor device manufacturing method in accordance with the present invention further comprises the step of etching the antireflection film with the hard mask.

Thus, at least one of the antireflection film and barrier metal layer can be etched by use of the same mask as that used for the metal film. This simplifies the manufacturing process.

A semiconductor device according to the present invention comprises a substrate, a MIS type element, a metal

wiring, and a hard mask. The MIS type element has an electrode provided such that an insulating film is arranged between this electrode and the substrate. The metal wiring has a predetermined pattern and is provided on the MIS type element by way of an interlayer insulating film. The hard mask is arranged on the metal wiring conductor and has a predetermined pattern identical to that of the metal wiring. The metal wiring conductor is connected through a conduction path to the electrode of the MIS type element.

A semiconductor device according to the present invention comprises a substrate, a MIS type field-effect transistor, a metal wiring, and a hard mask. The MIS type field-effect transistor has a source, a drain and a control electrode. The source and drain are arranged on the substrate. The control electrode is capable of controlling a current flowing between the source and the drain, and is arranged such that an insulating film is provided between the control electrode and the substrate. The metal wiring has a predetermined pattern and is provided on the MIS field-effect transistor by way of an interlayer insulating film. The hard mask is provided on the metal wiring and has a predetermined pattern identical to that of the metal wiring. The metal wiring is connected to a conduction path to the control electrode of the MIS type field-effect transistor.

This semiconductor device can be made by the semiconductor device manufacturing method mentioned above.

Brief Description of the Drawings

The present invention can easily be understood when the following detailed description is taken into consideration with reference to the accompanying drawings, which are represented only by way of example, wherein:

Fig. 1A is a sectional view of a semiconductor device manufactured on a substrate by employing the semiconductor device manufacturing method in accordance with the present invention, whereas Fig. 1B is a plan view associated with the sectional view in the step shown in Fig. 1A;

Fig. 2A shows a sectional view in a step in which a photoresist mask has been formed in order to form a mask pattern to a hard mask film, whereas Fig. 2B shows a sectional view in a step in which the hard mask has been formed;

Fig. 3A shows a sectional view in a step in which metal wiring has been formed by etching the metal film using the hard mask, whereas Fig. 3B shows a plan view in a step in which the metal wiring has been formed by etching the metal film;

Fig. 4 is a sectional view in a step in which a passivation film has been formed;

Fig. 5A is a schematic view showing the distribution of both of the electrified charge in an etching step by use of the hard mask and the electric charge induced by this electrified charge, whereas Fig. 5B is a schematic view showing the distribution of both of electrified charge in

an etching step by use of the photoresist and electric charge induced by the electrified charge;

Fig. 6A is a diagram showing, in terms of capacitors, the distribution of both of electrified charge in an etching step by use of the photoresist and electric charge induced by the electrified charge, whereas Fig. 6B is a diagram showing, in terms of capacitors, the distribution of both of electrified charge in an etching step by use of the hard mask and electric charge induced by the electrified charge; and

Fig. 7 is a graph showing the experimental results of time-dependent dielectric breakdown (TDDB), which is one of methods for evaluating the deterioration of the gate oxide film.

Best Modes for Carrying Out the Invention

Preferred embodiments of the present invention will now be described in detail with reference to the drawings. Parts identical to each other will be referred to with the same reference numerals or letters, if possible, to avoid their redundant description.

Fig. 1A is a sectional view showing a semiconductor device, which is being manufactured by a method of manufacturing a semiconductor device, of an embodiment of the present invention; whereas Fig. 1B is a plan view corresponding to the sectional view in the manufacturing step shown in Fig. 1A. Fig. 1A corresponds to the cross

sectional view taken along the line I-I of Fig. 1B.

In the following, a method of manufacturing a semiconductor device comprising a metal wiring on a metal-insulator-semiconductor type (MIS type) semiconductor device will be described. This MIS type device means at least one transistor of a MIS type transistor having a control electrode and a MIS type capacitor. In the following configuration, manufacturing steps for forming a metal-oxide-semiconductor type (hereinafter referred to as "MOS type") field-effect transistor on a silicon substrate of p-type conductivity will be explained, but embodiments according to the present invention are not limited the configuration.

Referring to Figs. 1A and 1B, a device isolation film 4 is formed on the surface of a silicon substrate 2. The device isolation film 4 works as insulation regions for separating respective device regions 6 from each other in which the MOS transistor is formed. The device isolation film 4 is provided by forming an insulating film, such as a silicon oxide film, in the insulating regions. Methods for isolating devices, such as LOCOS method and LOPOS method, can be employed, but they are not limited thereto.

Subsequently, a polysilicon layer 8 is formed on the substrate 2. The polysilicon layer 8 is utilized as a conductive layer, such as a control electrode 8a on the device regions 6 and a wiring layer 8b on the device separation

film 4. The polysilicon layer 8 is formed by the following process. After a gate insulation film 10 is formed by use of thermal oxidation method, a polysilicon film is formed by CVD method thereon. This polysilicon film is etched to form a predetermined pattern.

In the device regions 6, n-type semiconductor regions 6a and 6b are formed. Each of the n-type semiconductor regions 6a and 6b is formed in a self-alignment manner with respect to the control electrode 8a and the device separation film 4. For example, ion implantation method can be employed for introducing the n-type impurity atoms, but it is not limited to the methods. One of the n-type semiconductor regions 6a and 6b act as a source region of a MOS type transistor, whereas the other acts as a drain region of the MOS type transistor. The n-type semiconductor regions 6a and 6b are separated from each other by the control electrode 8a. Provided between thus separated n-type semiconductor regions 6a and 6b is a channel region 6c. The gate oxide film 10 is arranged between the channel 6c and the control electrode 8a. Since the conductivity of the channel region 6c is modulated by the voltage applied to the control electrode 8a, the control electrode 8a acts as a gate electrode for controlling the current flowing between the source and drain regions.

Formed on the substrate 2 are the control electrode 8a, n-type semiconductor regions 6a and 6b for the source

and drain regions, and an interlayer insulating film 14. The MOS type transistor has the control electrode 8a, and the source and drain regions of the n-type semiconductor regions 6a and 6b. The interlayer insulating film 14 is utilized for electrically separating the control electrode 8a from a wiring layer formed thereon. The insulating film 14 is formed by the following process, for example. A predetermined thickness of BPSG film is deposited by use of CVD method. Thereafter, the BPSG film is flattened by a heat treatment.

Conductive portions are formed in the interlayer insulating film 14. The conductive portions electrically connects the source and drain regions of the n-type semiconductor regions 6a and 6b, the control electrode 8a, and the wiring layer 8b to the metal wiring formed in upper layers. In order to form the conductive portions, contact holes 12a, 12b, 12c, 12d are formed in the interlayer insulating film 14. The contact holes 12a, 12b, 12c, 12d are formed by the following process, for example. A photoresist mask having openings at predetermined positions is formed by use of photolithography method. Thereafter, the interlayer insulating film 14 at the openings is etched by plasma etching. This etching forms the contact hole 12a to the n-type semiconductor region 6a, whereby conductive portions can be formed and will connect the n-type semiconductor region 6a with the wiring layer. The contact

hole 12b is provided on the n-type semiconductor region 6b, whereby conductive portions can be formed and will connect the n-type semiconductor region 6b with the wiring layer. The contact hole 12c is provided on the wiring layer 8b, whereby a conductive portions can be formed and will connect the wiring layer 8b with the wiring layer. The contact hole 12d is provided on an extension of the control electrode 8a, whereby a conductive portion is formed and will connect the control electrode 8a and the wiring layer.

Fig. 2A is a sectional view in a manufacturing step after a photoresist having a mask pattern is formed on a hard mask film. Referring to Fig. 2A, a metal film 16 is deposited on the substrate 2. The metal film 16 is composed of a conductive film formed by at least one of conductive materials, such as aluminum, Al alloy, tungsten, and copper.

A barrier metal film may be provided under the metal film 16. Provided between the metal film 16 and the interlayer insulating film 14a is a barrier metal film made of a material, such as Ti or Ti/TiN. An antireflection film may be formed directly on the conductive film as well. The antireflection film can be made of p-SiON, TiN, Ti/TiN, Si, Si/TiN, p-SiON/TiN, and SiC, and can include a single-layer film having an organic coat film and a laminate film formed from materials selected from the materials listed above. Each of the barrier metal film, conductive film, and antireflection film can be formed, for example, by a

sputtering method or CVD method. The metal film 16 is also formed in the contact holes 12a, 12b, 12c and 12d provided in the interlayer insulating film 14 (see Fig. 1A). Conductive portions 16a, 16b, 16c and 16d (see Fig. 3B) are formed in the same step, and can be used to electrically connect the n-type semiconductor regions 6a and 6b, the control electrode 8b, and the wiring layer 8b to a metal film formed later thereon.

By way of example, the thickness of the metal film 16 is preferably at least 100 nm but not greater than 1000 nm in order to secure the characteristics and reliability of the resulting semiconductor device. In an example, The thickness of a Ti system barrier metal film:

at least 50 nm but not greater than 100 nm;

The thickness of a conductive film made of Al:

at least 100 nm but not greater than 1000 nm; and

The thickness of an antireflection film:

at least 50 nm but not greater than 100 nm.

Subsequently, a mask film 18 is formed on the metal film 16 and can be used as a hard mask. The hard mask film 18 can be a silicon system insulation film. For example, the silicon system insulation film can be a silicon inorganic film, such as SiO_2 film. This inorganic film is deposited by use of CVD method, for example.

Experiments carried out by the inventors found that the thickness of the hard mask film 18 is preferably at least

150 nm but preferably not greater than 300 nm in order to appropriately etch the metal film 16. The hard mask film 18 (acting as a hard mask 22) having the thickness of less than 150 nm cannot be used as a mask in etching the metal film 16. Namely, the film is too thin to be use as the mask if the thinning of film in the etching is taken into consideration during etching. If the thickness of the hard mask film 18 exceeds 300 nm, the breakdown and deterioration of the gate oxide film may become remarkable because the amount of charge increases in the etching. Therefore, the inventors carried out experiments and studies and finally found out this preferable range. The inventors conducted detailed studies of the experimental data. The studies reveals that the film thickness is further preferably at least 180 nm and further preferably not greater than 230 nm.

In addition, it is advantageous that the hard mask 22 of a silicon system inorganic film is not required to be removed after the metal wiring 24 has been formed.

After the deposition of these layers 16 and 18, the hard mask is formed by photolithography method, for example. Fig. 2B is a sectional view showing a manufacturing step in which the hard mask 22 has been formed. The hard mask 22 can be formed according to the following process. First, a photoresist is applied onto the hard mask film 18 and is exposed to light, whereby a wiring pattern for metal wiring

is transferred to form a resist layer 20. The hard mask film 18 is etched using this resist layer 20 as a mask. By way of example, conditions for etching the hard mask film 18 are listed below:

the flow rate for CHF_3: 10 sccm;

the flow rate for CF_4: 20 sccm;

the flow rate for Ar: 60 sccm;

the flow rate for O_2: 5 sccm;

the pressure within the chamber: 60 mTorr; and

the power: 200 Watts.

Such conditions are used for etching the hard mask film 18 to form the hard mask 22.

Subsequently, the metal film is etched using thus formed hard mask 22 as a mask. This etching process can be carried out by use of an etching apparatus, such as plasma etching apparatus. When the metal film 16 is thus etched by use of the hard mask 22, the breakdown and deterioration of the gate oxide film 10 are reduced during the etching.

Fig. 3A is a sectional view showing a manufacturing step in which the metal lines 24 has been formed after etching the metal film 16 by use of the hard mask 22. Fig. 3A is a sectional view taken along the line II-II of Fig. 3B. Fig. 3B is a plan view showing a manufacturing step in which the metal lines 24 has already been formed by etching the metal film 16. These drawings show the metal lines and hard mask

having the same pattern.

Referring to Fig. 3B, the control electrode 8a and the wiring layer 8b have a conductive path to the metal layer 16. The conductive path is provided by the conductive portion 16d formed within the contact hole 12d. After etching, the control electrode 8a and the wiring layer 8b have a conductive path to the metal lines 24. Therefore, when the metal lines 24 are exposed to the plasma for etching, the potential of the control electrode 8a and the wiring layer 8b are different from that of the substrate 2 even after the control electrode 8a and the wiring layer 8b have been formed. This potential corresponds to the amount of charge contained in the etching mask. The details thereof will be explained later.

After the metal lines 24 have been formed, a passivation film 26 is formed without removing the hard mask 22. Fig. 4 is a sectional view showing a manufacturing step in which the passivation film 26 has been formed. The passivation film 26 is formed and the structure of the passivation film 26 is composed of, for example, a silicon oxide film (PSG) doped with a low concentration of phosphorus (P) deposited by use of CVD method and a plasma nitride film formed thereon.

A semiconductor device is completed by the semiconductor device manufacturing method according to the embodiment of the invention. Although the semiconductor device in this embodiment has a single metal wiring layer 24, the present invention is also applicable to semiconductor

device further comprising at least one metal wiring layer added onto the metal wiring layer 24 as a matter of course. In the latter configuration, another metal layer, hard mask film and photoresist mask should be formed. The additional layers correspond to the metal layer 16, the hard mask film 18, and the photoresist mask 20, respectively.

These layers may be formed in the same manner as in the above-mentioned method, but the formation thereof is not limited thereto. Thereafter, the separate hard mask film is etched using the separate photoresist mask as a mask, whereby the metal wiring layer is formed. The configuration prevents the breaking and deteriorating of the gate oxide film for the MOS type transistor during the etching as well.

Conditions for etching the metal film above will now be explained. The etching is carried out using a mixed gas of Cl_2 gas, BCl_3 gas and CHF_3 gas. The Cl_2 gas and BCl_3 gas are used as a main ingredient of the etching gas and the CHF_3 gas is used as an additive gas.

As for the etching conditions, the following process is preferable, for example. The substrate 2 is mounted on a susceptor of the etching apparatus. Thereafter, the pressure in the process chamber is reduced to about 5 to 30 mTorr, e.g., 12 mTorr. The gas flow rate valve is controlled so as to supply Cl_2 gas, BCl_3 gas and CHF_3 gas and their flow rates of Cl_2 gas, BCl_3 gas, and CHF_3 gas are 80 sccm (about 60% with respect to the total amount), 40

sccm (about 10%), and not greater than 15 sccm, respectively. These gases are mixed and thus obtained mixture is introduced into the chamber. A high-frequency power is applied to generate high-density plasma in the chamber and is maintained. The plasma dissociates and ionizes the etching gas to create active species and ions of chlorine (Cl). The active species and ions mainly contribute to the etching of the metal film 16. Since the susceptor is applied to a negative potential, Cl ions advance toward the susceptor, thereby enabling the anisotropic etching in a direction normal to the susceptor.

The mixing ratio of Cl_2 gas and BCl_3 gas can be similar to that as conventionally employed for an etching gas for the metal film. Although Al metal and Al alloys are exemplified as material for the metal film 16 in the embodiment, any conductive material capable of being etched by the above-mentioned Cl-containing etching gas may be employed as a wiring material as well.

With reference to Figs. 5A and 5B, we will explain the mechanism allowing the reduction of the breakdown of the gate oxide film (the control electrode) of the MOS type transistor in forming the metal wiring. Fig. 5A is a schematic view showing both of electrified charge in the etching by use of the hard mask and electric charge induced in the metal film by the electrification charge. Fig. 5B is a schematic view showing both of electrified charge in the etching by use of the photoresist and electric charge

induced by the electrification charge. The inventors assume this mechanism as follows.

With the hard mask 22, the thickness of the hard mask is allowed to be smaller than that of a photoresist mask 23 when the metal film 16 of a predetermined thickness is etched. For example, the thickness of the photoresist 23 may be at least 1 μm but not greater than 2 μm. Although the etching of the metal film 16 requires the thickness of the photoresist to fall within the above range, the metal film 16 can be favorably etched by use of the hard mask 22 having a film thickness falling within a predetermined range as already described. Preferably, the thickness of the hard mask 22 falls within the range of at least 150 nm but not greater than 300 nm.

The hard mask 22 allows the reduction of the volume of the mask member in which the electrification occurs. Thus, the amount of charge in the mask member is reduced in the etching, and the amount of induced charge in the mask member can also be reduced as well. Further, experiments carried out by the inventors have revealed that further favorable results can be obtained when the film thickness of the hard mask 22 is at least 180 nm but not greater than 230 nm.

In the etching, the mask member accumulates electric charges so as to be charged negative, whereas the conductor to be etched is relatively charged positive because etchant ions reaching the metal film 16 are positive charge.

Consequently, the potential of the metal film 16 is different from that of the substrate 2.

Namely, since the control electrode (8a in Fig. 1A) and the wiring layer (8b in Fig. 1A) are electrically connected through connection paths (e.g., 16c and 16d in Fig. 2B) to the metal film, a potential difference occurs between the control electrode 8a and wiring layer 8b, and the substrate 2 opposed to them. The control electrode 8a is insulated from the substrate 2 by way of the thin gate insulating film 10, and the dielectric breakdown of the gate insulating film 10 occurs when the potential difference between the control electrode 8a and the substrate 2 increases above the predetermined value. In contrast, the dielectric breakdown does not occur in this embodiment because the amount of charge in the mask member is not large.

The photoresist 23 electrified with negative charge causes the phenomenon of shading, whereby electrons in the plasma 40 are bounced off (44 in Fig. 5B). However, in addition to the fact that the amount of charge in the hard mask 22 decreases, the hard mask 22 has advantages in the following points. With the hard mask 22, the aspect ratio can be smaller as compared with the conventional photoresist 23. With a small aspect ratio, electrons in the plasma 40 can reach a deeper region being etched (42 in Fig. 5A) because electrons in the plasma 40 are not bounced off by shading. The electrons having reached the metal film 16 in etching

can reduce the amount of positive charge in the metal film 16. As a consequence, the hard mask 22 also acts to reduce the electrification of the metal film 16 occurring in etching.

As can be seen from Figs. 5A and 5B, the method explained in this embodiment reduces not only the electric charge in the films in etching but also the electric charge induced by that electric charge. The inventors presume that a grater electrification of the mask member may occur in the regions of higher wiring density. However, the method according to this embodiment mentioned above provides two mechanisms to reduce the electrification in the mask member even in the high wiring density regions.

Fig. 6A is a diagram showing, by use of capacitors, both of the electrification charge in etching using the photoresist and the electric charge induced by the electrification charge. Fig. 6B is a diagram showing, by use of capacitors, both of the electrification charge upon etching using the hard mask and the electric charge induced by the electrification charge.

Referring to Fig. 6A, a greater amount of electrification charge exists because the photoresist 23 has a greater film thickness. Referring to Fig. 6B, a smaller amount of electrification charge exists because the hard mask 22 has a smaller film thickness. As a consequence, the potential difference V_1 between nodes A and B becomes greater than the potential difference V_2 between nodes C and D in

terms of the absolute value.

In Figs. 6A and 6B, a capacitor C1 is provided between the substrate 2 and a polysilicon layer 8 (e.g., reference numeral 8b in Fig. 1B) on the device separation film 4. A capacitor C2 is provided between the substrate 2 and a polysilicon layer 8 (e.g., reference numeral 8a in Fig. 1B) on the gate oxide film 10. The thickness of the gate oxide film 10 is smaller than that of the device separation film 4. The relationship C1 < C2 is obtained where the symbols C1 and C2 are their respective capacitance values per unit area.

A voltage across the capacitors C1 and C2, as shown in Fig. 6A, is higher than that across the capacitors C1 and C2, as shown in Fig. 6B. Since the thickness of the gate oxide film 10 is smaller than that of the device separation film 4, there is a larger likelihood of the occurrence of the gate oxide defects in the manufacturing process. That is, the defects may occur due to dielectric breakdown when a considerably high voltage is applied across the gate oxide. This phenomenon causes the breakdown of the control electrode (gate electrode) 8a.

Fig. 7 is a graph showing measurements of time-dependent dielectric breakdown (TDDB), which is a method for evaluating the deterioration in the gate oxide film.

In this method, samples are prepared as follows. Until the etching of an Al film (metal film) is completed, a

predetermined condition is maintained. The predetermined condition is: a process gas containing Cl_2, BCl_3 and CHF_3 that have respective flow rates of 60 sccm, 90 sccm, and 15 sccm, flows in the process chamber so as to keep a pressure of 10 mTorr. After the barrier metal layer has been etched, the next predetermined condition is maintained for 10 seconds. The next predetermined condition is as follows: a process gas containing Cl_2, BCl_3, and CHF_3 flows in the process chamber so as to keep a pressure of 7 mTorr, and that their respective flow rates are 30 sccm, 45 sccm, and 15 sccm. In the sample, the thickness of the gate oxide film is 4.5 nm and the gate area is 10 μm^2 and the film thickness of the hard mask is 150 nm.

Fig. 7 shows results of measurement for the samples prepared under the above conditions. In this measurement, a constant-current of 500 mA/cm^2 is applied to the control electrode of the samples, and the interval of time until each sample breaks is measured. In the graph of Fig. 7, the abscissa and ordinate indicate time and cumulative fraction defective, respectively. Data for the samples prepared by use of the photoresist are indicated by whitened circles, symbol "○", whereas those prepared by use of the hard mask are indicated by black circles, symbol "●". For comparison, whitened squares, the symbol "□", indicate data measured for samples having a control electrode connected to a simple electrode pattern (with an area which is 100,000 times the

control electrode area) which is not shaped in wiring. In the simple electrode pattern, no damages occur due to the shading because it is not a wiring pattern.

As shown in the graph of Fig. 7, the cumulative fraction defective is improved for the hard mask samples as compared with the results obtained for the photoresist samples. The result for the hard mask is substantially on a par with the result showing no damages due to the shading phenomenon.

As explained in the foregoing in detail with reference to the drawings, in carrying out plasma dry etching of a wiring layer electrically connected to the control electrode of a MOS type semiconductor device, the present invention can reduce the occurrence of the dielectric breakdown and deterioration in the gate oxide film due to the electrification of the wiring film accelerated in the high density wiring regions. The present invention is not limited to the embodiments, and is applicable to other semiconductor device manufacturing methods of forming a predetermined pattern of metal wiring connected through a conduction path to a control electrode provided on an insulating layer.

Industrial Applicability

As explained in the foregoing, the present invention employs a hard mask instead of a photoresist. The hard mask is utilized as a mask in forming a wiring layer connected through a conductive path to a control electrode. The hard mask makes it possible to reduce its initial film thickness

required for etching the metal film.

The thinner hard mask reduces the volume of the mask member, and thus decreases a portion of the mask member capable of capturing the electric charge during the etching process. This reduces the amount of electric charges in the mask member, whereby the voltage applied between the control electrode and the substrate can be lowered.

Thus provided are a method of manufacturing a semiconductor device and the semiconductor device, which can reduce the occurrence of the breakdown and deterioration in a gate oxide film in forming metal wirings on a control electrode of the semiconductor device.

CLAIMS

1. A method of manufacturing a semiconductor device said method forming metal wirings of a predetermined pattern connected through a conduction path to a control electrode on an insulating layer formed on a substrate, said method comprising the steps of:

forming a metal film;

forming, on said metal film, a hard mask with a film thickness of at least 150 nm but not greater than 300 nm, said hard mask containing a silicon system inorganic insulating film, and said hard mask having said predetermined pattern; and

etching said metal film with said hard mask by use of an etching gas to form metal wiring of said predetermined pattern;

wherein, in said step of forming said metal wiring, the amount of electric charge in said metal film is decreased to reduce the occurrence of the breakdown and deterioration, caused by said electric charge flowing into said control electrode, of said insulating layer.

2. A method of manufacturing a semiconductor device according to claim 1, wherein said hard mask is made of silicon oxide.

3. A method of manufacturing a semiconductor device

according to claim 1 or 2, wherein said metal film is at least one of an Al film and an Al alloy film.

4. A method of manufacturing a semiconductor device according to claim 1 or 2, wherein said metal film is at least one of a tungsten film and a copper alloy film.

5. A method of manufacturing a semiconductor device according to any one of claims 1 to 4, wherein said hard mask has a film thickness of at least 180 nm but not greater than 230 nm.

6. A method of manufacturing a semiconductor device according to any one of claims 1 to 5, wherein a barrier metal film is formed.

7. A method of manufacturing a semiconductor device according to claim 6, further comprising the step of etching said barrier metal film by use of said hard mask.

8. A method of manufacturing a semiconductor device according to any one of claims 1 to 7, wherein an antireflection film is provided between said metal film and said hard mask.

9. A method of manufacturing a semiconductor device according to claim 8, further comprising the step of etching

said antireflection film by use of said hard mask.

10. A method of manufacturing a semiconductor device according to claim 1, wherein said etching gas contains Cl.

11. A method of manufacturing a semiconductor device having metal wirings of a predetermined pattern, said method comprising the steps of:

forming, on an insulating layer, a control electrode for a metal-insulator-semiconductor type device;

forming a metal film connected through a conduction path to said control electrode;

forming, on said metal film, a hard mask with a film thickness of at least 150 nm but not greater than 300 nm, said hard mask having said predetermined pattern and containing a silicon type inorganic insulating film; and

etching said metal film with said hard mask by use of an etching gas to form metal wiring of said predetermined pattern.

12. A method of manufacturing a semiconductor device according to claim 11, further comprising the step of forming said insulating film prior to forming said control electrode on said insulating layer.

13. A method of manufacturing a semiconductor device

according to claim 11 or 12, further comprising the step of forming a source and a drain for said metal-insulator-semiconductor type device.

14. A method of manufacturing a semiconductor device according to any one of claims 11 to 13, wherein said hard mask is made of silicon oxide.

15. A method of manufacturing a semiconductor device according to any one of claims 11 to 14, wherein said hard mask has a film thickness of at least 180 nm but not greater than 230 nm.

16. A method of manufacturing a semiconductor device according to any one of claims 11 to 15, further comprising the steps of:

forming a barrier metal film prior to forming said metal film; and

etching said barrier metal film by use of said hard mask.

17. A method of manufacturing a semiconductor device according to any one of claims 11 to 16, further comprising the steps of:

forming an antireflection film on said metal film prior to forming said hard mask on said metal film; and

etching said antireflection film by use of said hard mask.

18. A semiconductor device comprising:

a substrate;

a MIS type device having an electrode provided on an insulating film between said electrode and said substrate;

a metal wiring layer provided on said MIS type device by way of an interlayer insulating film, said metal wiring layer having a predetermined pattern; and

a hard mask, provided on said metal wiring layer, having a predetermined pattern identical to that of said metal wiring layer;

wherein said metal wiring layer is electrically connected to said electrode of said MIS type device.

19. A semiconductor device comprising:

a substrate;

a MIS type transistor having a source and a drain provided on the substrate; and a control electrode for controlling a current flowing between said source and drain, said control electrode being provided on an insulating film, said insulating film being provided between said control electrode and said substrate;

a metal wiring layer provided on said MIS type transistor by way of an interlayer insulating film, said

metal wiring layer having a predetermined pattern; and

a hard mask, provided on said metal wiring layer, having a predetermined pattern identical to that of said metal wiring layer;

wherein said metal wiring layer being electrically connected to said control electrode of said MIS type transistor.

20. A semiconductor device according to claim 19, wherein said MIS type field-effect transistor is a MOS type field-effect transistor.

ABSTRACT

The present invention provides a method of manufacturing a semiconductor device which is capable of reducing the occurrence of the breakdown and deterioration of a gate oxide film for a control electrode in forming a metal wiring on a semiconductor device having a control electrode. The semiconductor device manufacturing method forms metal wirings 24 of a predetermined pattern connected through a conduction path to a control electrode 8a on an insulating layer 10 formed on a substrate 2. The method comprises the steps of: (1) forming a metal film; (2) forming, on the metal film, a hard mask 22 with a film thickness of 150 nm to 300 nm, said hard mask 22 having the predetermined pattern and comprising a silicon type inorganic insulating film; and (3) etching the metal film by an etching gas with the hard mask 22 to form metal wirings 24 of the predetermined pattern, thereby, lowering the amount of electric charge electrifying the metal film. This method prevents the breakdown and deterioration of the insulating layer due to the electric charge flowing into the control electrode. More preferably, the film thickness of the hard mask 22 is 180 nm to 230 nm.

Fig.1A

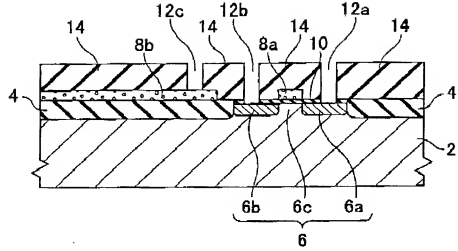
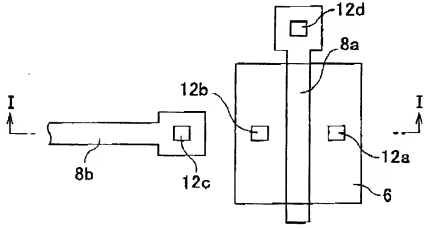

14
12c
12b
14
12a
14
8b
8a
14
10
4
4
2
6b
6c
6a
6

Fig.1B


12d
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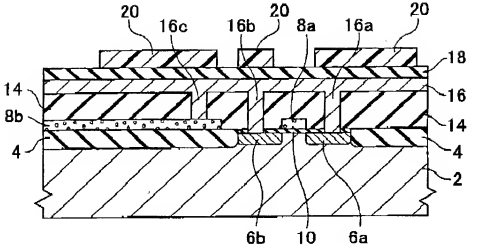
12b
I
I
12a
8b
12c
6

Fig.2A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16a
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8b
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6b
10
6a

Fig.2B

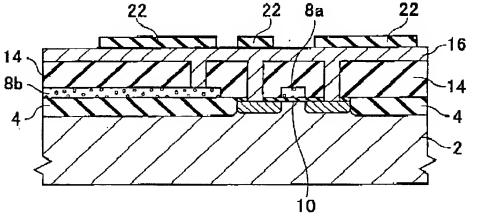
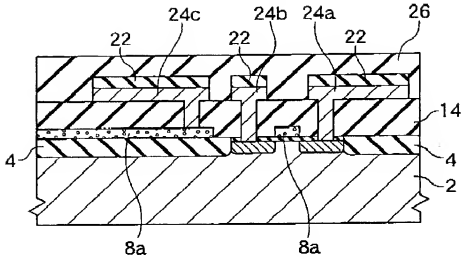

22
22
8a
22
16
14
8b
14
4
4
2
10

Fig.4



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Combined Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

This declaration is of the following type:

[ ] original [ ] supplemental

[X] national stage of PCT

[ ] divisional [ ] continuation [ ] continuation-in-part

My residence, post office address and citizenship are as stated next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF MANUFACTURING SEMICONDUCTOR DEVEICE

the specification of which

[ ] is attached hereto.

[X] was filed on November 7, 2001
as United States Application Serial Number 10/030525 and,
was amended on _____ (if applicable).

[X] was filed on May 2, 2000
as PCT International Application Number PCT/JP00/02914 and,
was amended under PCT Article 19 on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims as amended by any amendment referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATIONS, BENEFIT CLAIMED UNDER 35 USC §119(a)

Application Number	Country	Date of Filing (Day/Month/Year)	Priority Claimed Under 35 USC 119
P1999-127688	Japan	07 / May / 1999	[X] Yes [ ] No
			[ ] Yes [ ] No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

PRIOR U.S. PROVISIONAL APPLICATIONS, BENEFIT CLAIMED UNDER 35 USC §119(e)

(Application No.)	(Filing Date)	(Application No.)	(Filing Date)
(Application No.)	(Filing Date)	(Application No.)	(Filing Date)

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PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S., BENEFIT CLAIMED UNDER 35 USC §120

(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Combined Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

This declaration is of the following type:

[ ] original [ ] supplemental

[X] national stage of PCT

[ ] divisional [ ] continuation [ ] continuation-in-part

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Attorney's Docket No SEI/P016

Combined Declaration and Power of Attorney

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			[ ] Yes [ ] No

I hereby claim the benefit under Title 35 United States Code Section 119(e) of any United States provisional application(s) listed below.

PRIOR U.S. PROVISIONAL APPLICATIONS, BENEFIT CLAIMED UNDER 35 USC §119(e)

(Application No.)	(Filing Date)	(Application No.)	(Filing Date)
(Application No.)	(Filing Date)	(Application No.)	(Filing Date)

I hereby claim the benefit of Title 35, United States Code Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS
DESIGNATING THE U.S., BENEFIT CLAIMED UNDER 35 USC §120

(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number or Customer Number)

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Keith M. Tackett	Registration No. 32,008
Douglas H. Elliot	Registration No. 32,982
W. Bruce Patterson	Registration No. 34,102
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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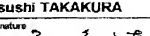
Fifth inventor's signature 	Date July 8, 2002
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Attorney's Docket No SOEI/0016

Combined Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

This declaration is of the following type:

[ ] original [ ] supplemental

[X] national stage of PCT

[ ] divisional [ ] continuation [ ] continuation-in-part

My residence, post office address and citizenship are as stated next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF MANUFACTURING SEMICONDUCTOR DEVEIGE

the specification of which

[ ] is attached hereto.

[X] was filed on November 7, 2001
as United States Application Serial Number 10/030525 and,
was amended on _____ (if applicable)

[X] was filed on May 2, 2000
as PCT International Application Number PCT/JP00/02914 and,
was amended under PCT Article 19 on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1 56

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed

PRIOR FOREIGN APPLICATIONS, BENEFIT CLAIMED UNDER 35 USC §119(a)

Application Number	Country	Date of Filing (Day/Month/Year)	Priority Claimed Under 35 USC 119
P1999-127688	Japan	07 / May / 1999	[X] Yes [ ] No
			[ ] Yes [ ] No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

PRIOR U.S PROVISIONAL APPLICATIONS, BENEFIT CLAIMED UNDER 35 USC §119(e)

(Application No.)	(Filing Date)	(Application No)	(Filing Date)
(Application No.)	(Filing Date)	(Application No)	(Filing Date)

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PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U S , BENEFIT CLAIMED UNDER 35 USC §120

(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)

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